HDPYX 160 & 230 - G

G-Series, ultimate performance in global shutter

1.6 and 2.3 Megapixel, Global Shutter HDR CMOS image sensor











The HDPYX-G image sensors use a groundbreaking global shutter pixel with dual in-pixel memory to capture prefect high dynamic range (HDR) images. Outstanding features are excellent in-scene dynamic, low noise and high sensitivity. The result is a perfect picture in all conditions. Target applications and market include scanning, night vision, ITS, robotic and surveillance.

Key Features

Global shutter pixel for easy use Build-in pixel high-dynamic technology Monochrome and RGB-Nir Micro-lenses for higher efficiency Square pixels Very high MTF in NIR range

Artefact free HDR processing
Digital CDS for black level constancy
Two low noise 11bits ADC
Pixel processing pipeline (ISP)
8/10/12/14/16bits output format
Linear and compressed mode

8 regions of interest (ROI) Sequencer Context meta data GPIO for trigger and status Master and slave modes

Mirror and flip Subsampling and binning up to x4

MIPI CSI-2 output (4 Lanes / 800Mbps)
Parallel output (12bits / 100 MHz)
Serial communication interface

Integrated temperature sensors Safety features

Model	HDPYX 160- <i>G</i>	HDPYX 330-G
• Resolution Class	1.6 Megapixel	2.3 Megapixel
 Active Pixels 	1472 x 1104	1944 x 1204
 Aspect Ratio 	4:3	16:10
• Frame Rate	75 fps	60 fps
 Optical Diagonal 	1/3" / 5.9mm	1/2.5" / 7.3mm

Pixel Performance

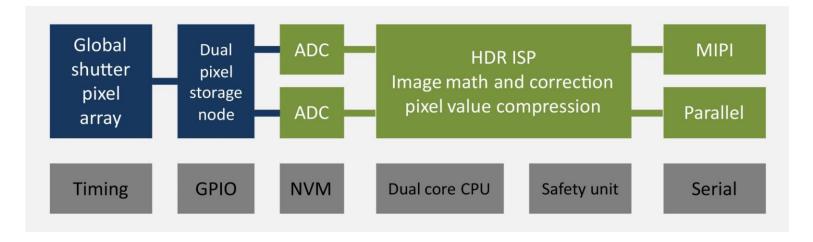
- 3,2µm pitch
- Linear Dynamic range up to 98 dB
- Single integration with 72dB de DR
- Saturation capacity (Full Well) 2 x 7.1ke-
- QE 69% at 550nm and 19% at 850nm
- SNR Max 41.6dB
- Noise of 2.1 e- RMS (60°C)
- Dark current of 21.75 e-/s (60°C)

Environment

- Low power design
- Operating temperature of -40°C to 125°c
- Automotive qualified IM2BG4 plastic package
- Automotive qualification AEC-Q100 grade 2
- ASIL B Compliant
- BGA or bare die available



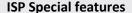




Operation modes

The sensor can work in Linear mode with up to 11 bits per pixels

HDR image capture is done in two phases:
A <u>short</u> and a <u>long</u> exposure in a sequence without noticeable timing gap. The pixel uses two storage nodes for the results. Charges accumulated in long and short timing storage nodes are converted in parallel though a double 11bits ADC. The 22bits result is processed in the image processing unit (ISP) and formatted to a 16bits HDR value.



Background removal in combination with an illumination source to get higher contrast in pattern projection systems.

Compression from 18 to 8bits for a logarithmic response Digital correction artefacts like hot pixels.

